## 3.1 A 14b 20mW 640MHz CMOS CT ΔΣ ADC with 20MHz Signal Bandwidth and 12b ENOB

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Many applications, such as wireless and wireline communication, medical imaging, and high-performance video, demand analog-to-digital conversion with a signal bandwidth of several MHz and a resolution of 12 to 14b. Because of their lower power consumption and intrinsic anti-alias filtering CT ΔΣ modulators are ideally suited for such applications [1]. In contrast, both SC ΔΣ modulators and pipelined converters suffer from linearity impairment caused by sampling switches operating at the reduced supply voltages of deep-submicron CMOS technologies. In this paper, a 3rd-order CT ΔΣ modulator is proposed that uses a 4b quantizer and NRZ DAC pulse shaping with quantizer excess loop delay compensation. It achieves an ENOB of 12b at a 20MHz signal bandwidth. The ADC delivers 14b data at 20 to 40MS/s and depending on the input reference clock the loop filter is automatically tuned to different sampling frequencies.

The CT ΔΣ modulator architecture is shown in Fig. 3.1.1. In order to save power and maintain a signal-transfer function (STF) with a good anti-aliasing filter characteristic, a combination of feedforward and feedback stabilized loop filter is implemented [2]. The feedback path to the input of the second integrator is replaced by the feedforward path $k_{4ff}$ to eliminate one DAC. A 620MHz full-scale interferer at the input of the modulator is filtered by the continuous-time loop filter and by the noise-transfer function (NTF) and results in a 20MHz alias that is -78dB below the full-scale signal. The feedback parameter $k_{zfb}$ in Fig. 3.1.1 introduces a resonator loop that creates a notch in the NTF that further reduces the quantization noise within the signal band [3].

The loop filter is realized as an active RC filter (see Fig.3.1.3). Due to the low supply voltage and the high-linearity requirement (THD<-78dB) multi-stage opamps with feedforward $G_m$-C compensation and Class-AB output stages are used [4], as shown in Fig. 3.1.2. To overcome the conditional stability of this multi-stage structure, the feedforward paths are designed such that the lowest order path saturates last. When the opamp is overdriven, it thus reduces to an unconditionally stable system. The first integrator contains a 4-stage opamp which dissipates 1.2mW in the first differential pair to satisfy the thermal-noise requirement. Three-stage opamps are used for the second and third integrator stages, as these stages have more relaxed requirements. Trimming of integrator time constants is accomplished by digitally programming binary weighted capacitor arrays with switches. The data for the switches are generated by a trimming circuit which compares a replica of the RC time constant to the period of the input reference clock. Thus, the modulator can operate automatically in a range of 20 to 40MS/s output data rate. The input of the loop filter is resistive and therefore, no extra buffer amplifiers are needed, which are necessary to drive the input of SC modulators.

To maintain stability generic CT ΔΣ modulators require a small time delay of the quantizer compared to the sampling period. In this design, the quantizer delay is set to half of the sampling period and a feedback path, $k_{3fb}$, from the quantizer output to the input is added to achieve an equivalent system, as shown in Fig. 3.1.1 [1]. Hence, the requirement regarding delay for the quantizer is relaxed and the overall power consumption is reduced. As the effect of the quantizer delay is already considered during the development of the modulator system, a more aggressive NTF can be realized and a lower stability margin can be tolerated. DAC1 realizes $k_{1fb}$, DAC2 is used to realize $k_{2fb}$ and together with DAC3 it is used to realize $k_{3fb}$, the direct feedback around the quantizer (see Fig. 3.1.3). The idea behind the implementation of the direct feedback path is first to introduce a differentiation and then to feed the signal to the last integrator. This results in a frequency independent feedback and an additional summing amplifier is avoided. The differentiation is carried out by subtracting from the feedback signal of DAC2 a delayed version of the output of DAC3 by half a clock period later. In effect a signal that is proportional to the derivative of the quantizer output and has RZ pulse shaping is applied to the last integrator, as shown in Fig. 3.1.4.

The 15 comparators of the internal Flash-ADC consist of a double differential input stage and a regenerative latch. To reduce capacitive loading of the loop filter the comparators use minimum size input transistors and a trimming circuit compensates the device offsets during the start up.

All three current steering DACs have 4b of resolution and use NRZ pulse shaping. A careful differential design in conjunction with the reduced-swing high-crossing differential switching scheme sufficiently minimizes the clock feedthrough, glitch energy and inter-symbol interference. Thus no RZ pulse shaping that would increase sensitivity to clock jitter is necessary.

The linearity requirement of THD<-78dB for the first DAC results in a considerable area requirement. To ease wiring between quantizer and DAC cells, the cells are arranged in a linear array. To counter thermal and mechanical gradients, the even numbered cells in ascending order are interleaved with the odd numbered cells in descending order. Additionally, special care is taken in the routing of the ground network to achieve the same voltage drops in the supply rails of all 15 current source transistors.

The CT ΔΣ modulator is implemented in a 0.13μm 1-poly 8-metal CMOS technology in an area of 1.2mm². The chip micrograph is shown in Fig. 3.1.7. At an OSR of 16 ($f_{clk}$=640MHz) it converts a signal bandwidth of 20MHz while consuming 20mW from a 1.2V supply. Up to a input signal frequency of 19.5MHz values for SNR, THD, and SINAD are 76dB, -78dB, and 74dB, respectively. To ease board-level integration a VGA, bandgap reference, and a clock multiplying LC-PLL are integrated on the same die as well as the decimation filter. The LC-PLL generates the sampling clock with 300fs rms jitter and provides a clock clean-up function because of its bandwidth of 450kHz.

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*References:*
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[2] F. Munoz et al., "A 4.7mW 89.5dB DR CT Complex ΔΣ ADC with Built-In LPF," *ISSCC Dig. Tech. Papers*, pp. 500-501, Feb., 2005.
[3] S. R. Norsworthy, R. Schreier, and G. C. Temes, "Delta-Sigma Data Converters: Theory, Design, and Simulation," IEEE Press, 1996.
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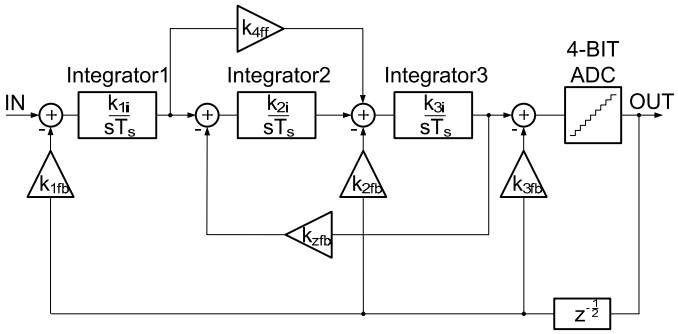


Figure 3.1.1: Continuous-time ΔΣ modulator architecture.

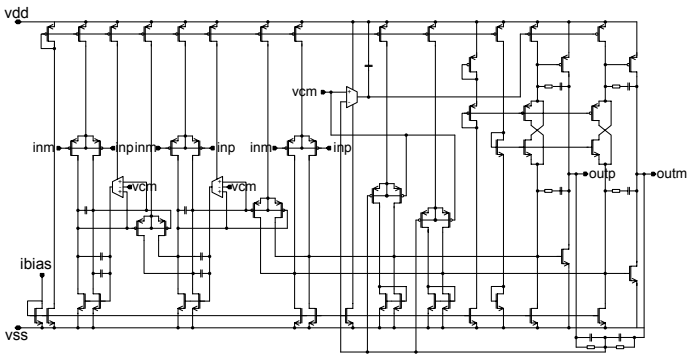


Figure 3.1.2: Multi-stage opamp with feedforward $G_m$-C compensation.

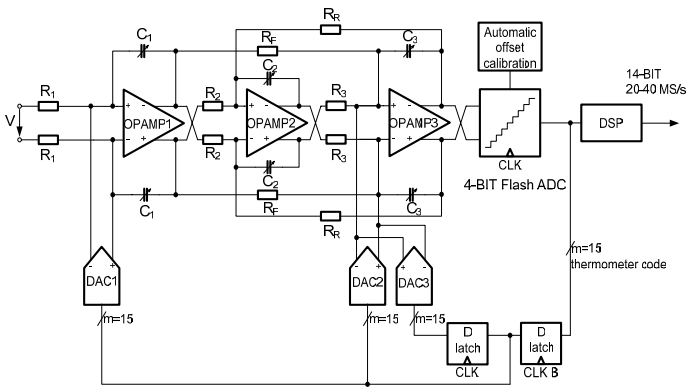


Figure 3.1.3: Continuous-time ΔΣ modulator.

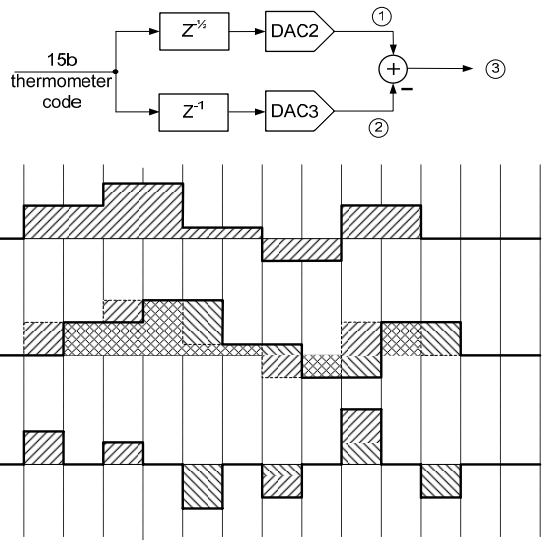


Figure 3.1.4: Generation of the RZ pulse-shaped derivative of the quantizer output.

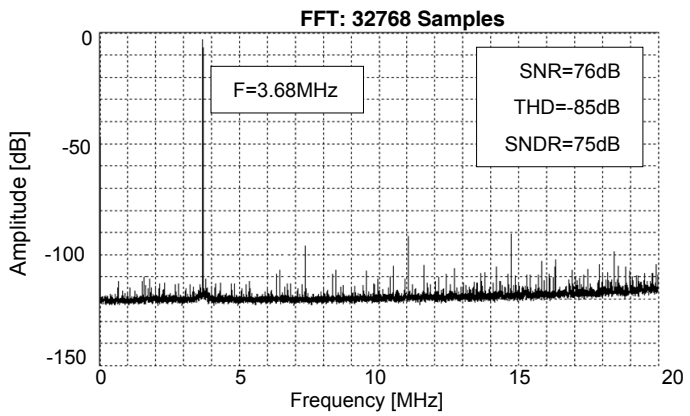


Figure 3.1.5: Measured output spectrum.

| | | |
|---|---|---|
| Sampling Frequency | | 640MHz |
| Conversion Rate | | 40MS/s |
| Signal Bandwidth | | 20MHz |
| Peak SNR @3.68MHz | | 76dB |
| THD@3.68MHz | | -78dB |
| Peak SNDR@3.68MHz | | 74dB |
| Peak SNR @ 10MHz | | 76dB |
| THD@10MHz | | -78dB |
| Peak SNDR @10MHz | | 74dB |
| ENOB | | 12 |
| Power | Modulator 640MHz | 20mW |
| | Decimator 40MS/s | 18mW |
| | PLL 2.56GHz | 12mW |
| | VGA | 15mW |
| | I/O 1.8V | 4mW |
| Power Supply | | 1.2V |
| Process | | 130nm 1P8M CMOS |
| Chip Area | | 8.6mm$^2$ |

Figure 3.1.6: Performance summary.

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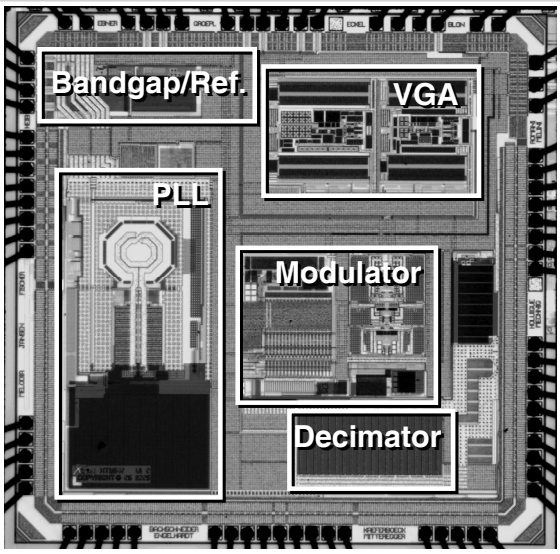


**Figure 3.1.7: Chip micrograph.**